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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,061	03/12/2004	Eitan Cadouri	524322001200	6747

56702 7590 01/09/2006

PDF SOLUTIONS c/o MOFO SF
425 MARKET STREET
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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,061	CADOURI, EITAN	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: in line 3 of the claim, the limitation "a die placement" should be change to --said die placement-- in order to avoid a duplicant positive recitation for the limitation in the claim. Appropriate correction is required.

2. Claim 2 is objected to because of the following informalities: in line 1 of the claim, the limitation "a die placement" should be change to --said die placement-- in order to avoid a duplicant positive recitation for the limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 1, 8, and 14, the claims state: "...the die placement defines the locations on the wafer on which the dies are to be fabricated..." In viewing the specification, it is neither clear nor concise that the die placement defines the locations on the wafer. It appears that the tester head defines the location on the wafer, which the dies are fabricated. Further, the specification does not clearly described that the dies are going to be fabricated as claimed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al (6640423) in view of admitted prior art.

Regarding claim 1, Johnson et al disclose a method of selecting a die placement of dies (dies 26) on a wafer (substrate 48) to reduce test time of the dies, the method comprising: a) obtaining [via computers 55 and 66] a die placement (die holder 100) of dies (26) on the wafer (48), b) determining placements [via computers 55 and 66 and positioning device 24] of a tester head (probe 604) needed to test the dies (26) in the die placement (100); c) determining [via computers 55 and 66] a number of touchdowns needed in the determined placements of the tester head (604), wherein a touchdown involves lowering the tester head (604) to form an electrical contact between pins on the tester head (604) and bonding pads [not number but shown] on a die (26) being tested; and d) adjusting the die placement (100) [via position device 24 and control device 22] to reduce the number of touchdowns. However, they do disclose die placement defines the locations on the wafer as claimed. The admitted prior art discloses that it is well known to use the die placement to define the location on the wafer, which the dies are to be fabricated [see page 1, paragraphs [0003]-[0004] for details]. It would have been well known and obvious to a person having ordinary skill in the art at the time the invention was made to have the die placement in Johnson et al to define the location on the wafer since the prior art teaches

that having the die placement to define the location on the wafer helps track the locations of the dies that fail or have low yield during testing.

Regarding claim 2, Johnson et al disclose wherein steps b) to d) are iterated to obtain a die placement (100) with a minimum number of touchdowns needed to test the dies (26) in the die placement.

Regarding claim 3, Johnson et al disclose the placements of the tester head (604) are determined based on a test program [via computers 55 and 66].

Regarding claim 4, Johnson et al disclose wherein steps a) to d) are iterated for different test programs [via computers 55 and 66] to determine a combination of die placement and test program with a minimum number of touchdowns.

Regarding claim 5, Johnson et al disclose wherein steps a) to d) are iterated for different tester heads (604) to determine a combination of die placement (100), test program, and tester head with a minimum number of touchdowns.

Regarding claim 6, Johnson et al disclose steps a) to d) are iterated for different tester heads to determine a combination of die placement (100) and tester head (604) with a minimum number of touchdowns.

Regarding claim 7, Johnson et al disclose the tester head (604) is configured to simultaneously test a set of multiples dies (26).

Regarding claim 8, Johnson et al disclose a method of selecting a die placement of dies (dies 26) on a wafer (substrate 48) to reduce test time of the dies, the method comprising: a) obtaining [via computers 55 and 66] a die placement (die holder 100) of dies (26) on the wafer (48), b) obtaining [via computers 55 and 66] a configuration of a tester head (probe 604) used to

test the dies (26) on the wafer (48); c) determining placements [via computers 55 and 66 and positioning device 24] of a tester head (probe 604) needed to test the dies (26) in the die placement (100); d) determining [via computers 55 and 66] a number of touchdowns needed in the determined placements of the tester head (604), and e) adjusting the die placement (100) [via position device 24 and control device 22] to reduce the number of touchdowns. However, they do disclose die placement defines the locations on the wafer as claimed. The admitted prior art discloses that it is well known to use the die placement to define the location on the wafer, which the dies are to be fabricated [see page 1, paragraphs [0003]-[0004] for details]. It would have been well known and obvious to a person having ordinary skill in the art at the time the invention was made to have the die placement in Johnson et al to define the location on the wafer since the prior art teaches that having the die placement to define the location on the wafer helps track the locations of the dies that fail or have low yield during testing.

Regarding claim 9, Johnson et al disclose wherein steps b) to d) are iterated to obtain a die placement (100) with a minimum number of touchdowns needed to test the dies (26) in the die placement.

Regarding claim 10, Johnson et al disclose the placements of the tester head (604) are determined based on a test program [via computers 55 and 66].

Regarding claim 11, Johnson et al disclose wherein steps a) to d) are iterated for different test programs [via computers 55 and 66] to determine a combination of die placement and test program with a minimum number of touchdowns.

Regarding claim 12, Johnson et al disclose wherein steps a) to d) are iterated for different tester heads (604) to determine a combination of die placement (100), test program, and tester head with a minimum number of touchdowns.

Regarding claim 13, Johnson et al disclose steps a) to d) are iterated for different tester heads to determine a combination of die placement (100) and tester head (604) with a minimum number of touchdowns.

Regarding claim 14, Johnson et al disclose a system (system 10) of selecting a die placement (die holders 100) of dies (dies 26) on a wafer (substrate 48) to reduce test time of the dies, the system (10) comprising: an initial die placement (100) of dies (26) on the wafer (48) [via positioning device 24], a tester head (probe 604) having pins to contact bonding pads on a die (26) on the wafer (48) being tested; and an adjusted die placement (die holders 76), wherein the adjusted die placement (76) is derived from the initial die placement (100) by determining placements of the tester head (604) needed to test the dies (26) on the initial die placement (100) and a number of touchdowns needed in the determined placements of the tester head (604), and wherein the adjusted die placement (76) requires fewer touchdowns by the tester head (604) to test the dies (26) on the adjusted die placement than the dies (26) on the initial die placement (100). However, they do disclose die placement defines the locations on the wafer as claimed. The admitted prior art discloses that it is well known to use the die placement to define the location on the wafer, which the dies are to be fabricated [see page 1, paragraphs [0003]-[0004] for details]. It would have been well known and obvious to a person having ordinary skill in the art at the time the invention was made to have the die placement in Johnson et al to define the location on the wafer since the prior art teaches that having the die placement to define the

location on the wafer helps track the locations of the dies that fail or have low yield during testing.

Regarding claim 15, Johnson et al disclose the initial die placement (100) and the adjusted die placement (76) have the same number of dies.

Regarding claim 16, Johnson et al disclose the tester head (604) is configured to simultaneously test a set of multiples dies (26).

Conclusion

7. Applicant's arguments filed Oct. 27, 2005 have been fully considered but they are not persuasive.

a) Regarding the claim objection, the applicant argues: "...Note, however, that the die placement obtained in step a) is not necessarily the same as the die placement referred to in the preamble..."

In response to the above statement, if the die placements are different, the examiner will like to suggest to applicant to change the claim language to show they are different by saying one die placement as first die placement and the other as second die placement. Further, if the die placements are different which die placement in step b is being referred too. Therefore, the examiner is maintaining the claim objection as well as the position that there is only one die placement in the claims until the applicant clearly distinguishes between different dies placements.

b) The applicant argues: "... the "die placement" recited in claims 1, 8, and 14 are non-analogous to the placement of dies referred to in the Johnson reference."

In response to applicant's argument that Johnson et al reference is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (517) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
January 6, 2006